REMARKS

Claims 1, 19, 32 and 41 have been amended. New claims 92-109 have been added to round out the scope of protection afforded by the invention. Claims 1-44 and 92-109 are pending in this application.

Claim 41 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. (Office Action at 4). In particular, the Office Action asserts that there is insufficient antecedent basis for the limitation "said silicide layer" recited in claim 41. In response, claim 41 has been amended to depend on claim 40, which in turn depends on claim 35. Applicants note that claim 35 recites the limitation "silicide layer" and, thus, the limitation "said silicide layer" in claim 41 has antecedent basis. Withdrawal of the rejection of claim 41 is respectfully requested.

Claims 1-4 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by Gardner et al. (U.S. Patent No. 6,255,698) ("Gardner '698"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a low-loss coplanar waveguide. As such, amended independent claim 1 recites a method of forming a coplanar waveguide by *inter alia* "forming a signal conductor line over a substrate" and "forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line." Amended independent claim 1 further recites "subsequently forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line."

Gardner '698 relates to a method of forming "an integrated circuit in which gate structures for n-channel and p-channel transistors are separately optimized." (Col. 1, lines 10-13). According to Gardner '698, "a p-type active region 12 and n-type active region 14

[are] formed within substrate 10." (Col. 8, lines 1-2; Fig. 1). Gardner '698 teaches that "[a]ctive region 12 may be separated from active region 14 and other adjacent active regions by isolation regions 16." (Col. 8, lines 3-4; Fig. 1). Gardner '698 also teaches that a "gate dielectric layer 18 is formed over the upper surface of substrate 10" and "[c]onductive . . . layer 22 is formed above dielectric 18." (Col. 8, lines 4-7; Fig. 1). Gardner '698 further teaches that "a conductive diffusion barrier layer 20 is formed between gate dielectric 18 and conductive layer 22." (Col. 8, lines 8-9; Fig. 1). According to Gardner '698, "[g]ate structures are patterned from layers 18, 20 and 22" such that "[g]ate structure 24 is formed over p-type active region 12, and gate structure 26 is formed over n-type active region 14." (Col. 8, lines 60-63; Fig. 2). Thus, Gardner '698 teaches the formation of trench 16 *before* the formation of gate structures 24, 26.

Gardner '698 does not teach or suggest "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 1 recites (emphasis added). As noted above, Gardner '698 teaches that gate structures 24, 26, which would arguably correspond to the ground conductor plane of the claimed invention, are formed *before* and not *subsequently* to the formation of the isolation region 16, which would arguably correspond to the trench of the claimed invention. For at least these reasons, Gardner '698 does not anticipate the subject matter of claims 1-4 and 8, and withdrawal of the rejection of these claims is respectfully requested.

Claims 6, 7, 9, 16-19, 29-32 and 42-44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner '698. This rejection is respectfully traversed.

Claims 6, 7, 9 and 16-18 depend on amended independent claim 1, which recites *inter alia* "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and subsequently forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line." Claims 29-31 depend on amended independent claim 19, which recites *inter alia* "forming

at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and subsequently forming at least one trench . . . having a depth of about 100,000 Angstroms to about 200,000 Angstroms and a width of about 100,000 Angstroms to about 150,000 Angstroms." Claims 42-44 depend on amended independent claim 32, which recites *inter alia* "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and forming at least one trench in said silicon substrate by use of an isotropic etching process . . . said at least one trench having a radius of about 50,000 Angstroms to about 100,000 Angstroms."

The subject matter of claims 6, 7, 9, 16-19, 29-32 and 42-44 would not have been obvious over Gardner '698. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three requirements must be met: (1) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine reference teachings; (2) a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. More importantly, the teaching or suggestion to make the claimed combination and the reasonable expectation for success must both be found in the prior art and not based on Applicants' disclosure. See, e.g., In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

In the present case, not all claim limitations of amended independent claims 1, 19 and 32 are taught or suggested by the prior art. Gardner '698 does not teach or suggest "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 1 recites (emphasis added). Gardner '698 also fails to teach or suggest "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming at least one trench in said silicon substrate in an area between said at least one ground conductor plane and said signal

conductor line," as amended independent claim 19 recites (emphasis added).

Gardner '698 is also silent about "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and forming at least one trench in said silicon substrate *by use of an isotropic etching process*," as amended independent claim 32 recites (emphasis added). In fact, Gardner '698 is silent on the process by which its isolation region or trench is formed. For at least these reasons, the subject matter of claims 6, 7, 9, 16-19, 29-32 and 42-44 would not have been obvious over Gardner '687, and withdrawal of the rejection of these claims is respectfully requested.

Claims 10, 11, 20, 21, 23-26, 33, 34 and 36-39 stand rejected under 35 U.S.C. §103(a) as being obvious "over Gardner et al. (U.S. 6,255,698) in view [of] Gardner et al. (U.S. 6,255,698)." (Office Action at 32). Since the Gardner '698 patent was cited in view of itself, but the Office Action listed Garner et al. (U.S. Patent No. 6,140,688) as a second reference in the Notice of References Cited, Applicants infer that the rejection was intended to be based upon both "Gardner '698" and "Gardner '688." This rejection is respectfully traversed.

Gardner '688 teaches a method of forming "a semiconductor device having a self-aligned metal-containing gate structure." (Col. 1, lines 7-10). According to Gardner '688, a semiconductor substrate has "a transistor 11 formed in an active region 12 of a semiconductor substrate 10." (Col. 6, lines 10-13; Fig. 1). Gardner '688 teaches that "[a]ctive region 12 is separated from adjacent active regions by isolation regions 14" and that a "gate dielectric 16 and a gate structure including gate conductor 18 are formed above the active region." (Col. 6, lines 13-16; Fig. 1). Gardner '688 further teaches that isolation regions may be formed by methods such as "the formation of trenches which are subsequently filled with a deposited dielectric." (Col. 6, lines 26-29). According to Gardner '688, "[d]ielectric regions . . . are subsequently formed over the substrate and surrounding the transistor gate conductors." (Col. 2, lines 3-6). Thus, Gardner '688 also teaches the formation of the gate structures *after* the formation of the trench.

The subject matter of claims 10, 11, 20, 21, 23-26, 33, 34 and 36-39 would not have been obvious over Gardner '698 in view of Gardner '688, whether considered alone or in combination. Neither of Gardner '698 nor Gardner '688 teaches or suggests all limitations of amended independent claims 1, 19 and 32. Neither Gardner '698 nor Gardner '688 teaches or suggests "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 1 recites (emphasis added). As mentioned above, Gardner '698 teaches the formation of trench 16 *before* and not *subsequent* to the formation of gate structures 24, 26, as in the claimed invention.

In addition, neither Gardner '698 nor Gardner '688 teaches or suggests "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming at least one trench . . . having a depth of about 100,000 Angstroms to about 200,000 Angstroms and a width of about 100,000 Angstroms to about 150,000 Angstroms," as amended independent claim 19 recites (emphasis added). As noted above, Gardner '698 teaches the formation of a trench *before* and not *subsequent* to the formation of gate structures, as amended independent claim 19 recites. As also discussed above, Gardner '688 also teaches the formation of the gate structures *after* the formation of the trench.

Gardner '698 and Gardner '688, whether considered alone or in combination, also fail to teach or suggest "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and subsequently forming at least one trench in said silicon substrate *by use of an isotropic etching process* in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 32 recites (emphasis added). Gardner '698 teaches creation of isolation regions by forming trenches that are "subsequently filled with a deposited dielectric" or by "local oxidation of the substrate" which fails to form a trench at all. (Col. 8, lines 17-21). Similarly, Gardner '688 mentions the same methods of creating isolation regions. (Col. 6, lines 26-31). Both

Gardner '698 and Gardner '688 are silent on the "use of an isotropic etching process" to form a trench, as recited in amended independent claim 32. For at least these reasons, the subject matter of claims 10, 11, 20, 21, 23-26, 33, 34 and 36-39 would not have been obvious over Gardner '698 in view of Gardner '688, and withdrawal of the rejection of these claims is respectfully requested.

Claims 5, 12, 13, 22, 27, 28, 35, 40 and 41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner '698 in view of Gardner '688, and in further view of Filipiak (U.S. Patent No. 5,447,887) ("Filipiak"). This rejection is respectfully traversed.

Filipiak relates to a method of improving adhesion of silicon nitride to a copper surface "by the addition of an intervening copper silicide layer." (Col. 2, lines 17-19). Filipiak teaches that a "conductive plug 20 is formed within opening 16 to make contact to doped region 18." (Col. 2, lines 65-67; Fig. 2). According to Filipiak, "a second dielectric layer 22 . . . includes a plurality of openings 24" and that one of the openings "exposes conductive plug 20." (Col. 3, lines 10-13; Fig. 2). Filipiak also discloses that "a conductive layer 26 is deposited over the semiconductor device" and that the conductive layer is deposited such that "the sidewalls of dielectric layer 22 within opening 24 are coated, as is the top surface of conductive plug 20." (Col. 3, lines 40-45; Fig. 3). Filipiak further discloses that "a copper layer 28 is blanketly disposed over semiconductor device 10." (Col. 3, lines 48-49; Fig. 3). Filipiak teaches that "copper layer 28 . . . is polished back to form a plurality of copper interconnects 30 within openings 24." (Col. 4, lines 1-3; Fig. 4).

The subject matter of claims 5, 12, 13, 22, 27, 28, 35, 40 and 41 would not have been obvious over Gardner '698, Gardner '688 and Filipiak, whether considered alone or in combination. None of Gardner '698, Gardner '688 and Filipiak teaches or suggests "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line," as

amended independent claim 1 recites (emphasis added). Filipiak also fails to teach or suggest any of the limitations of amended independent claims 19 and 32. In fact, Filipiak does not mention the formation of a trench at all, much less the formation of a trench "in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 1 recites, for example. As mentioned above, Gardner '698 and Gardner '688 both teach the formation of a trench *before* and not *subsequent* to the formation of gate structures, as amended independent claim 1 recites. For at least these reasons, the subject matter of claims 5, 12, 13, 22, 27, 28, 35, 40 and 41 would not have been obvious over Gardner '698, Gardner '688 and Filipiak, and withdrawal of the rejection of these claims is respectfully requested.

Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner '698 in view of Hsue et al. (U.S. Patent No. 5,846,625) ("Hsue"). This rejection is respectfully traversed.

Hsue relates to a method for "manufacturing planar field oxide isolation structures on semiconductor substrate." (Col. 1, lines 15-18). Hsue teaches that a "silicon substrate 10 is subjected to an anisotropic[] etch . . . thereby forming in the substrate recessed areas 14 or trenches." (Col. 5, lines 8-10; Fig. 2). Hsue also teaches that a process is used "to selectively fill the recessed areas 14 in the silicon substrate 10 with silicon oxide . . . having a top surface which is coplanar with the principle surface of the silicon substrate 10." (Col. 5, lines 49-67; Col. 6, lines 1-45; Figs. 3 and 4). Hsue teaches forming a trench *and filling the trench* with silicon oxide *before* the formation of gate electrodes.

The subject matter of claims 14 and 15 would not have been obvious over Gardner '698 and Hsue, whether considered alone or in combination. Hsue and Gardner '698 do not teach or suggest "forming at least one longitudinal ground conductor plane . . . on a side of said signal conductor line . . . and *subsequently* forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line," as amended independent claim 1 recites (emphasis added). As mentioned

above, Gardner '698 teaches the formation of a trench *before* and not *subsequent* to the formation of gate structures, as amended independent claim 1 recites. Hsue also teaches trench formation *before* the formation of gate electrodes. For at least these reasons, the subject matter of claims 14 and 15 would not have been obvious over Gardner '698 and Hsue, and withdrawal of the rejection of these claims is respectfully requested.

A marked-up version of the changes made to claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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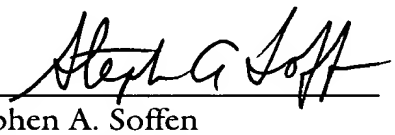
Respectfully submitted,

By 

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Version With Markings to Show Changes Made

1. (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a substrate;

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

subsequently forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line.

19. (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a silicon substrate;

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

subsequently forming at least one trench in said silicon substrate in an area between said at least one ground conductor plane and said signal conductor line, said at least one trench having a depth of about 100,000 Angstroms to about 200,000 Angstroms and a width of about 100,000 Angstroms to about 150,000 Angstroms.

32. (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a silicon substrate;

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

forming at least one trench in said silicon substrate by use of an isotropic etching process in an area between said at least one ground conductor plane and said signal conductor line, said at least one trench having a radius of about 50,000 Angstroms to about 100,000 Angstroms.

41. (Amended) The method of claim [41] 40, wherein said copper layer is exposed to silane at 300° C to form said silicide layer.